EECE 310 - Lecture 13

Outline

- Applications
- Graphical Analysis using Load Line

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- **Applications**
- Graphical Analysis using Load Line

Applications

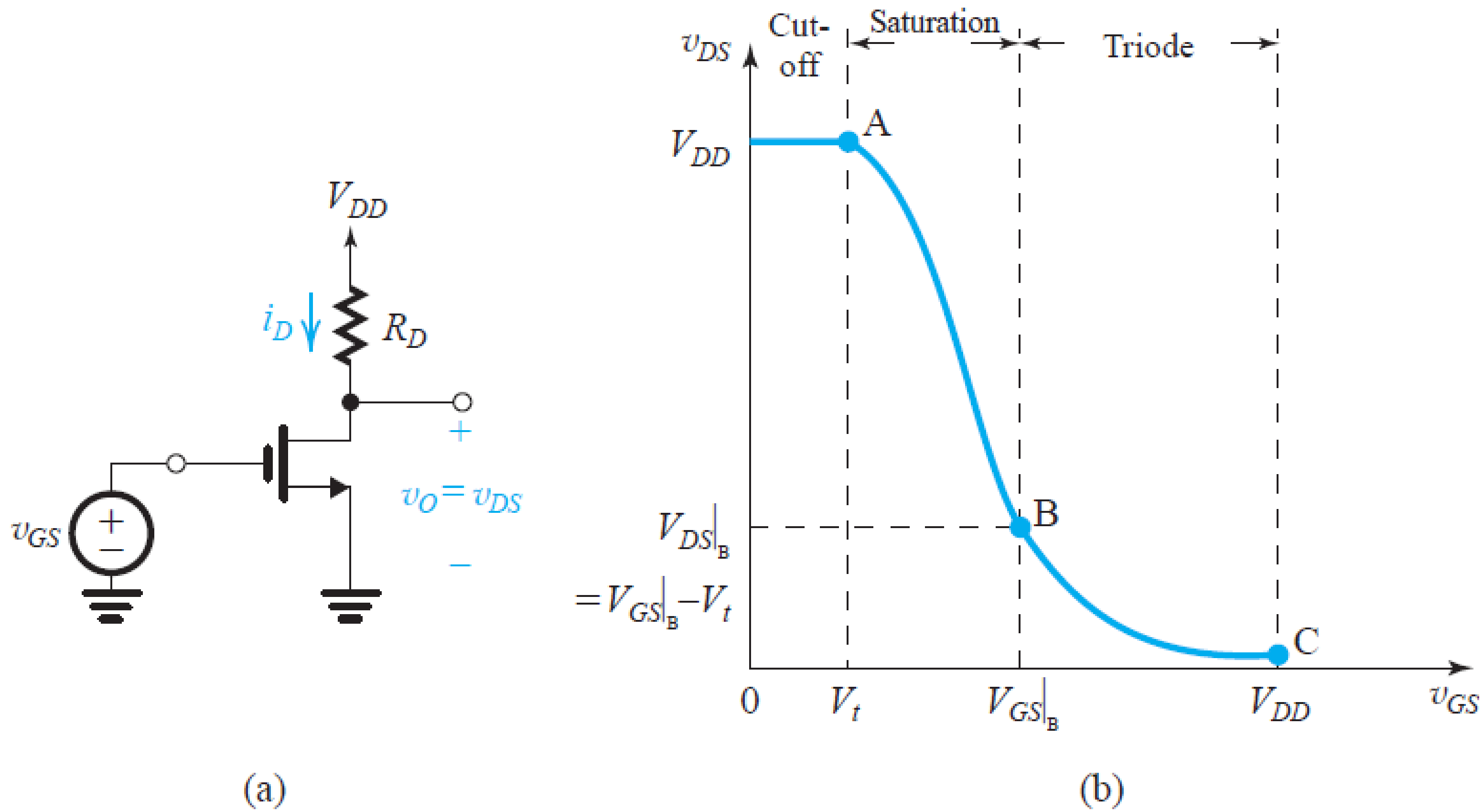


Figure 5.27 **(a)** Simple MOSFET amplifier with input v_{GS} and output v_{DS}. **(b)** The voltage transfer characteristic (VTC) of the amplifier in **(a)**. The three segments of the VTC correspond to the three regions of operation of the MOSFET.

Applications

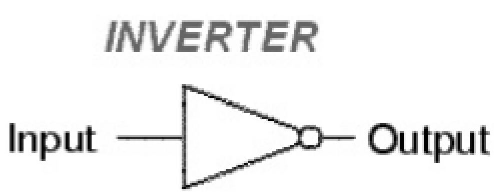
- **Application as an inverter (NOT gate)**

Digital application

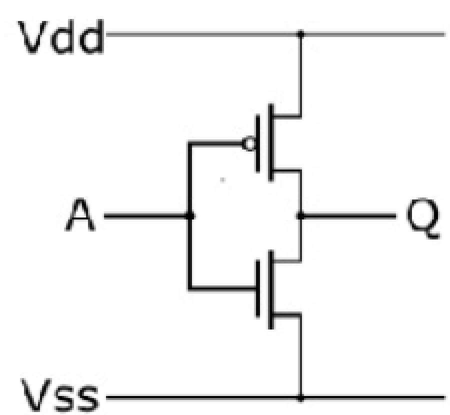
- In the MOSFET circuit:

Small voltage at V_I $(< V_t) \rightarrow V_O = V_{DD}$ $(large\ voltage)$

Large Voltage at V_I (close to V_{DD}) $\rightarrow V_O$ is very small

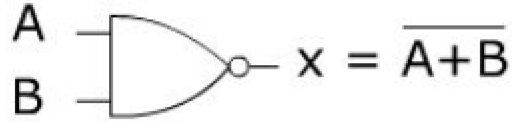


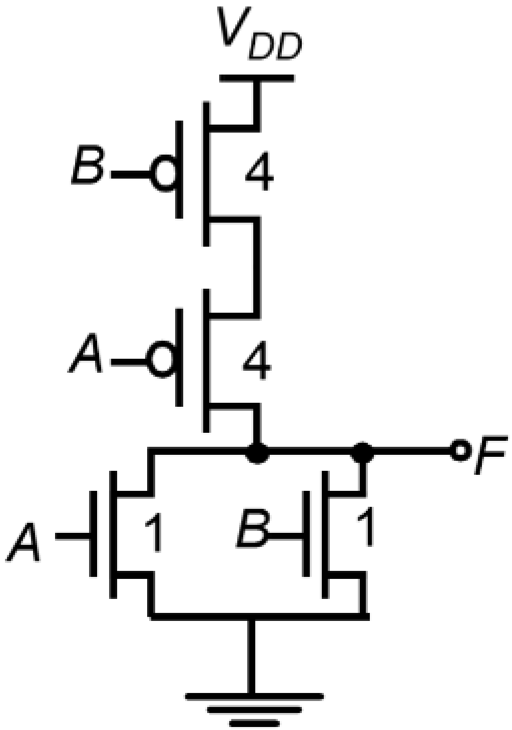
Input	Output
1	0
0	1



Applications

We can also build a NOR gate as follows:





Applications

Proper Biasing is the key:
MOSFET should be saturated with a good range for the voltage and a large gain.

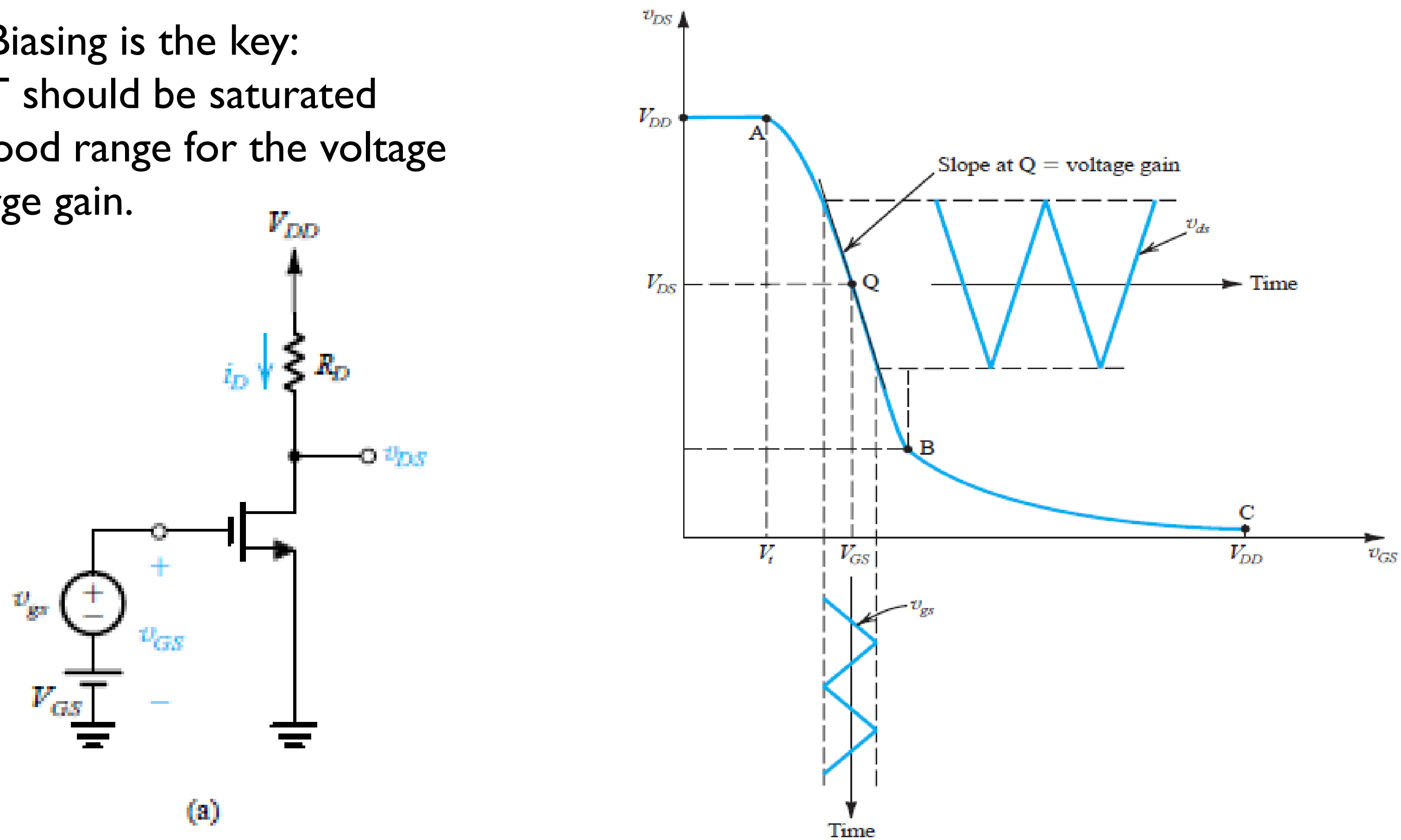


Figure 5.29 The MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS}. The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage $v_{ds} = A_v v_{gs}$.

Applications

- **Application as an Amplifier ANALOG:**

$$|Gain| = \frac{V_{opp}}{V_{ipp}}$$

$$Small\ signal\ gain = \frac{dv_o}{dv_i} \text{ at Q}$$

- In saturation: $V_O = V_{DD} - \frac{1}{2}Rk(V_I - V_t)^2$

$$\frac{dv_o}{dv_i} = -Rk(V_I - V_t)$$

At Q: $gain = -Rk\left(V_{IQ} - V_t\right) = -RkV_{oVQ}$

What are the limits to avoid distortion: A and B $\Rightarrow$ keep it in SAT

Limits in input:

$$V_{IQ} + V_{i(signal)max} \leq V_{1B}$$

$$V_{IQ} - V_{i(signal)max} \geq V_{1A}$$

Applications

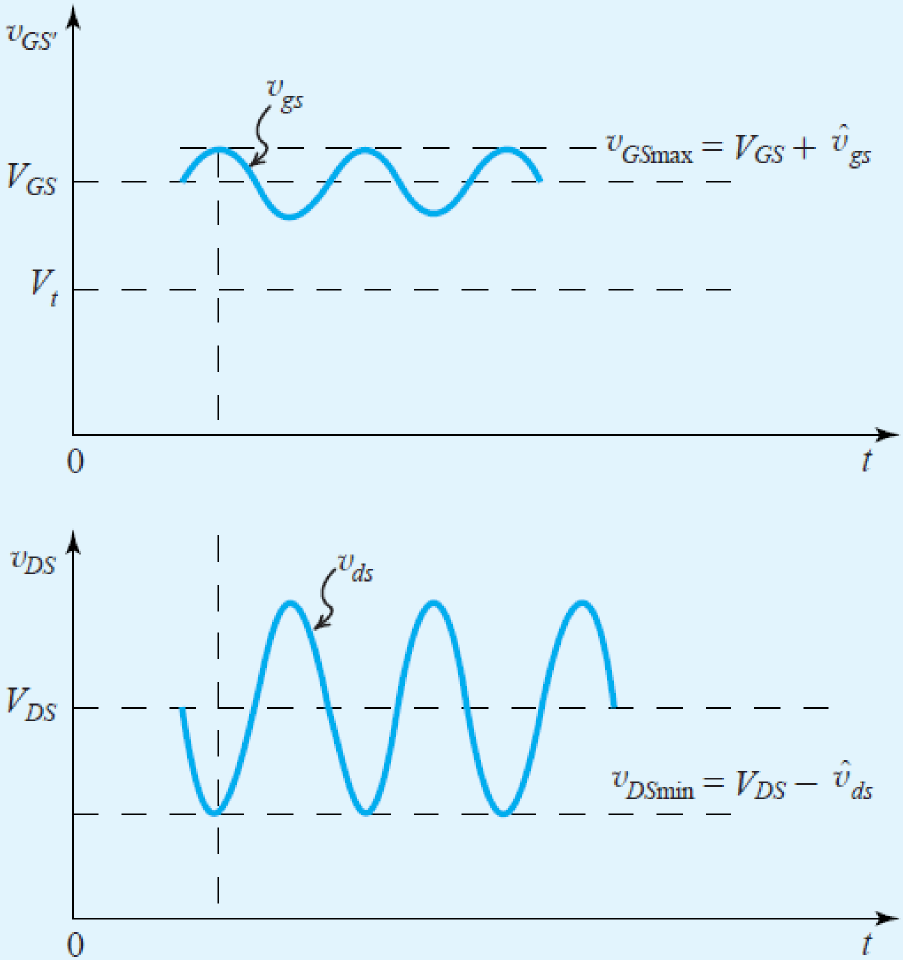


Figure 5.30 Signal waveforms at gate and drain for the amplifier in Example 5.9. Note that to ensure operation in the saturation region at all times, $v_{DSmin} \geq v_{GSmax} - V_t$.

Outline

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- **Graphical Analysis using Load Line**

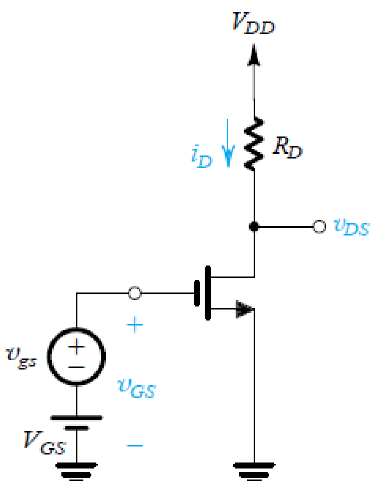
Graphical Analysis using Load Line

From circuit: $V_{DD} - R_D i_D - V_{DS} = 0$

Straight line called load line

→ $i_D = V_{DD}/R_D - V_{DS}/R_{DD}$

$$\rightarrow Slope = -\frac{1}{R_D}$$



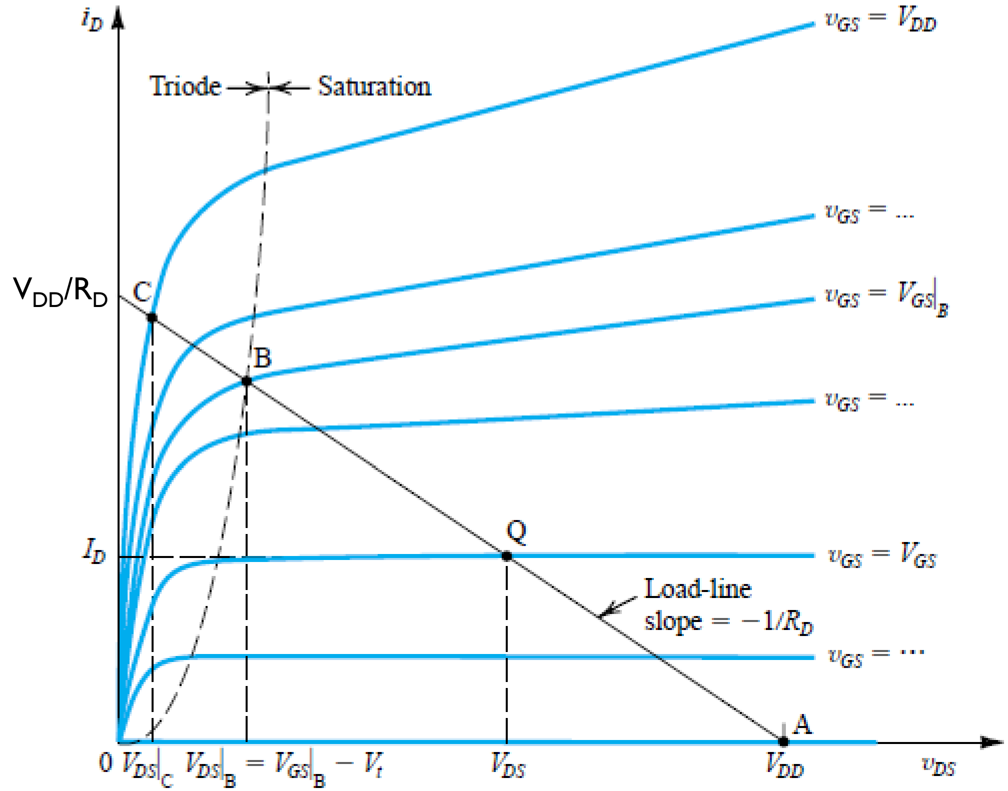


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

Graphical Analysis using Load Line

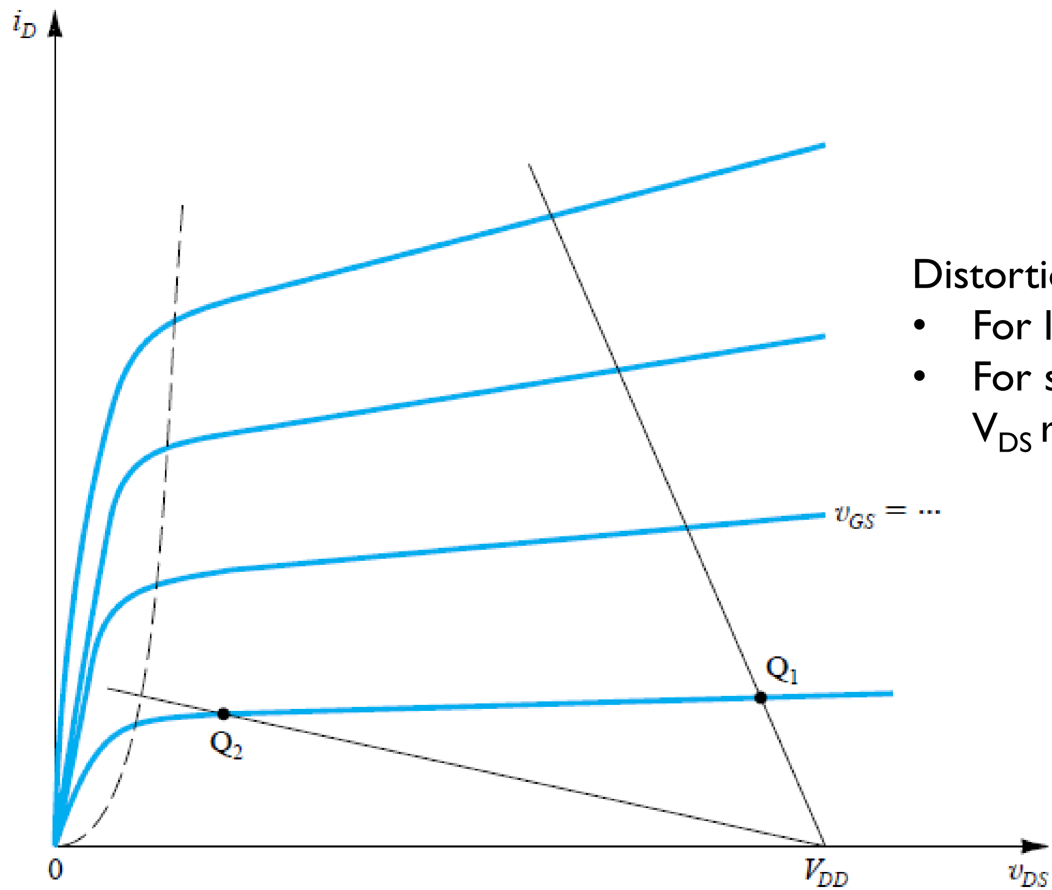


Figure 5.33 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

Effect of R_D

Distortion:
- For large R_D, MOSFET leaves SAT
- For small R_R, no room for swing as V_{DS} reach V_{DD}

Thank you !